

HIGHLY CONFIGURABLE PLL ARCHITECTURE  
FOR PROGRAMMABLE LOGIC

Abstract of the Disclosure

A programmable logic device includes configurable phase-locked loop (PLL) circuitry that outputs multiple clock signals having programmable phases and frequencies. Each output signal is programmably selectable for use as an external clock, internal global clock, internal local clock, or combinations thereof. The PLL circuitry has programmable frequency dividing, including programmable cascaded frequency dividing, and programmable output signal multiplexing that provide a high degree of clock design flexibility.